Listing of Claims:

Claims 1-28 (canceled).

29. (previously presented) A circuit, comprising:

a first capacitor having first and second terminals;

a second capacitor having first and second terminals, the first terminal of the second capacitor coupled to the second terminal of the first capacitor;

a first transistor coupled across the first capacitor; and

a second transistor coupled to the first transistor and across the second capacitor, wherein the first and second transistors are adapted to provide a bleed current to the first and second capacitors to balance a leakage current imbalance in the first and second capacitors.

30. (previously presented) The circuit of claim 29 further comprising a resistor divider network coupled to respective control terminals of the first and second transistors to define an input reference for the circuit.

31. (previously presented) The circuit of claim 30 wherein the resistor divider network comprises at least two resistors coupled to the respective control terminals of the first and second transistors.

32. (previously presented) The circuit of claim 29 wherein the first and second transistors are coupled to the second terminal of the first capacitor and the first terminal of the second capacitor, the first and second transistors adapted to maintain a voltage at the

second terminal of the first capacitor and the first terminal of the second capacitor within an input reference range.

33. (previously presented) The circuit of claim 29 wherein the bleed current is substantially equal to the leakage current imbalance in the first and second capacitors.

34. (previously presented) The circuit of claim 29 wherein the bleed current is substantially equal to zero when a voltage at the second terminal of the first capacitor and the first terminal of the second capacitor remains fixed at a voltage within an input reference range.

35. (previously presented) The circuit of claim 29 wherein the first and second transistors are coupled in a sink-source follower circuit configuration.

36. (previously presented) The circuit of claim 35 wherein the sink-source follower circuit is coupled to receive an input reference that is a fraction of a voltage between the first terminal of the first capacitor and the second terminal of the second capacitor.

37. (previously presented) The circuit of claim 36 wherein the input reference is a range of voltages including upper and lower reference voltages, each of which is offset from the fraction of the voltage between the first terminal of the first capacitor and the second terminal of the second capacitor.

38. (previously presented) The circuit of claim 37 wherein the offset of the upper and lower reference voltages from the fraction of the voltage between the first terminal of the first capacitor and the second terminal of the second capacitor is zero.

39. (previously presented) The circuit of claim 35 wherein the first and second transistors comprise bipolar junction transistors.

40. (previously presented) The circuit of claim 39 wherein the first and second transistors comprise a PNP transistor and an NPN transistor.

41. (previously presented) The circuit of claim 40 further comprising an impedance coupled to a collector of the first transistor to limit the bleed current through the first transistor.

42. (previously presented) The circuit of claim 29 wherein the circuit is an active circuit included in a power supply circuit.

43. (previously presented) The circuit of claim 41 wherein the impedance comprises a resistor.

44. (previously presented) The circuit of claim 40 further comprising an impedance coupled to a collector of the second transistor to limit the bleed current through the second transistor.

45. (previously presented) The circuit of claim 44 wherein the impedance comprises a resistor.